**April 12th Senior Project Update**

*Dhrvuit*:

* What I’ve Done Last Week
  + Get filter coefficients for a lowpass, highpass, bandpass (finished)
  + Look into mentor design checks and rules (working on it)
  + Get model data (next task)
* Goals for Upcoming Week
  + Get model data
  + Document Verilog code and Java model
* Blockers
  + None

*Julie*:

* Met with Dhruvit and reviewed progress and milestones that need to be accomplished in the EDA tool.
* Research towards the development of the resistor design using Pyxis layout and played around with the tools.

*Kevin*:

* What I’ve Done Last Week
  + Looked at tutorials of how to create a resistor in layout.
  + Began designing the resistor in layout
* Goals for Upcoming Week
  + Continue working on resistor layout
  + Determine types of layers needed
  + Verify resistor design
  + Create GDSII file
* Blockers
  + Found no tutorials for Mentor, only found tutorials for Cadence
  + Unsure of what layers to use for the resistor

*Whitley*:

* No report received

*Zach*:

* Goals for Past Week
  + Figure out what the “reset” warning means and if we can ignore it.
  + Further testing of the FPGA (maybe with filtering).
* What I Accomplished
  + I looked into the “reset” warning in more depth. First, I tried removing the reset signal from filter\_round\_truncate.v like Dhruvit previously did. I also found that the warning jumped to other modules. Next, I found a report online that claims this warning occurs when using an asynchronous reset and can be ignored. The report states “The above warning cites that while an RST signal was generated by the DCM, it does not drive clock pins such as flip-flop operations. This is because an asynchronous reset is used in the circuitry, and this does not pose any problem”. Next, I decided to test the reset signal on the FPGA. The reset signal is now defined from the red reset button on the FPGA. When the button is pressed, all of the outputs turn to zero. This means that the reset signal is reaching the submodule blocks. Overall, this makes me agree with the report I found and think that we can ignore the warning.
  + I recorded and verified the outputs of the FPGA test (passing audio stream through) in a FPGA Testing document. This document can be found at project\_asic/fpga/FPGA Testing.docx.
  + Filled in the Appendix sections of the final report.
  + Updated the website.
* Goals for Upcoming Week
  + Work with Whitley to get the I2C PSoC program interfaced with the FPGA.
  + Work with Whitley to test the I2C PSoC program.
  + Test the FPGA with filtering enabled
    - Using I2C if the PSoC program is working
    - If not, I will create separate projects with different default filter coefficient values.
* Blockers
  + Dhruvit needs to give me filter coefficient values for a couple different types of filters.
  + Dhruvit also needs to use his filter model to find what the output audio signal should be for the input audio signals that I sent him.